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ESL design apporach of Hw/Sw wireless devices based on a Virtual Platform/Network co-simulation environment

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Abstract

In this paper we focus on a simulation-based approach for the validation of both the architecture of a communicating object and its embedded software, interacting with other objects within a networked distributed system. This approach is based on co-simulation connecting the SystemC-TLM-based virtual prototyping tool Virtualizer from Synopsys and the network simulator OMNET ++. Exchanges between objects modelled under OMNET ++ create the stimuli to observe the behavior within the object modelled with Virtualizer. With the increase of embedded software in systems such as IoT, this approach allows to develop and validate at ESL a system platform and the application software in a virtualized environment.

Introduction

The design of wireless communicating devices requires to make the right choice of the hardware architecture to support within a reduced energy budget the execution of the functionality and the communication protocol, so as to achieve a desired quality of service. The move towards the Internet of Things imposes to consider inside the device higher processing capabilities and interaction facilities with a more generic/versatile architecture compared with current sensor devices in order to address a broader class of applications using this more generic platform. This objective leads to embed a MCU with the application and system software to support real-time processing and to allow the software to coordinate application, control, protocol and security activities within the device [1]. The IoT perspective considers also that end devices can perform upward and downward data/control communication not only to aggregate collected data but also to be able to control some process remotely. According to this perspective, the software part will have a more centric role in IoT devices and its development and debug will be more time consuming due to i) its embedded nature and ii), to the difficulties to anticipate the internal behaviour of the system included in a networked and distributed structure in which all the devices interact.

In this paper we illustrate that the joint use of a network simulator and a virtual prototyping tool in order to model in a single co-simulation environment both the distributed system structure and the internal architecture of the object with its the embedded software offers a convenient way to optimize at system level the hardware architecture and to develop/debug the system/application software.

Virtual platform model of the device

Synopsys proposes the SystemC-TLM oriented framework Virtualizer for the development of virtual prototypes where a virtual prototype can represent systems ranging from a processor core, system-on-chip or hardware board to electronic devices or a network of devices. These prototypes can be used throughout the specification, development and deployment of an electronic product [2].

In this work we use Virtualizer to model a ARC™ 625D [3] based platform. This SystemC-TLM model is developed at a register accurate level such

that the embedded software running on the ARC™ 625D core has the write hardware interface to interact with the slave modules connected on a AMBA bus. The architecture of our simple system is illustrated in Figure 1. Apart of the basic system components such as SRAM, Clock and Reset generators, a modem module and a thermal sensor component have been added in the architecture.

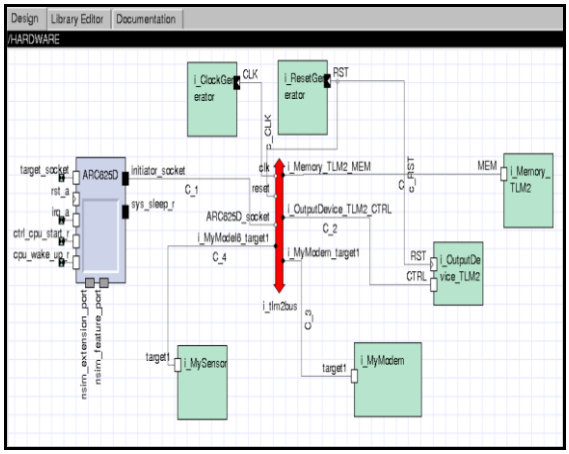

Figure 1. Internal architecture of the communicating object.

The modem module corresponds to the interface of a 802.15.4 device. In fact this slave component serves as a bridge to the network simulator. The thermal sensor is connected on the system bus as a slave and upon a read operation from the ARC™ 625D it provides the value of temperature of the CPU of the host machine on which Virtualizer is running.

The software running on the ARC™ 625D executes a simple scenario consisting in reading periodically the value from the thermal sensor and sending it through the modem interface to a coordinator node described in the OMENT++ network simulator. The binary code generated from the C software code using the ARC™ 625D compiler tool chain is loaded into the SRAM before starting the simulation.

Network model

OMNET++ is a well-known network simulator framework providing dedicated C++ libraries for modelling wired and wireless communication network with several networking protocols [4]. In this work we consider a simple network composed of five nodes connected through a 802.15.4 wireless protocol (
Figure 2). Each node in OMNET++ is structured as a set of functions corresponding to the application, network, MAC and physical layers with well-defined API between layers. The coordinator node[4] in Figure 2 corresponds to the SystemC-TLM model of the architecture given in Figure 1.

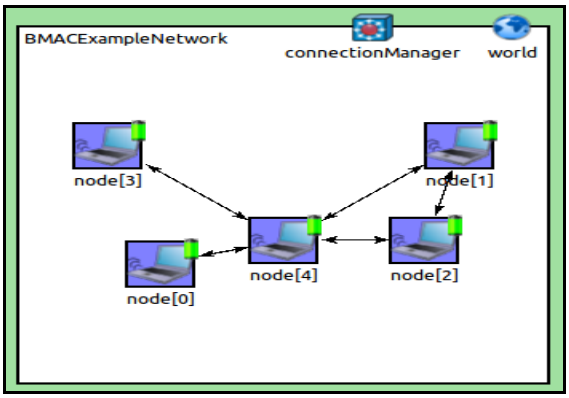

Figure 2. A simple network model in OMNET++

Virtual platform and network co-simulation

In this work we have particularized the node with ID [4] in
Figure 2 such that the application layer of this node is replaced in OMNET++ by the virtual platform model of the node developed with Virtualizer. To do this we have implemented a socket based communication mechanism between the modem module in the ARC™ 625D virtual platform and the application layer of that node in OMNET++. Each time the ARC™ 625D write a message in the modem, a connexion with OMNET++ is activated such that this message is routed from Virtualizer to OMNET++ and next through the layers of the node before it is sent to the coordinator. As soon as the message is broadcasted in the network, an acknowledgement is sent through the socket back to the modem module allowing the ARC™ 625D to send a new message.

Figure 3 gives some simulation results illustrating that the messages generated by the virtual platform are sent correctly to the network simulator. The message sent by the ARC™ 625D (the red box in upper part of Figure 3) through the modem module is well captured and processed by OMNET++ (red box of the lower part of Figure 3). Using this co-simulation approach, the interaction of a node with its environment and the impact of the environment on the behaviour of a node (Hw and Sw) can be evaluated and anticipated. Furthermore, power analysis due to the node activity can be performed using Virtualizer and power strategies can be developed to reduce power consumption of the system immersed in its environment.

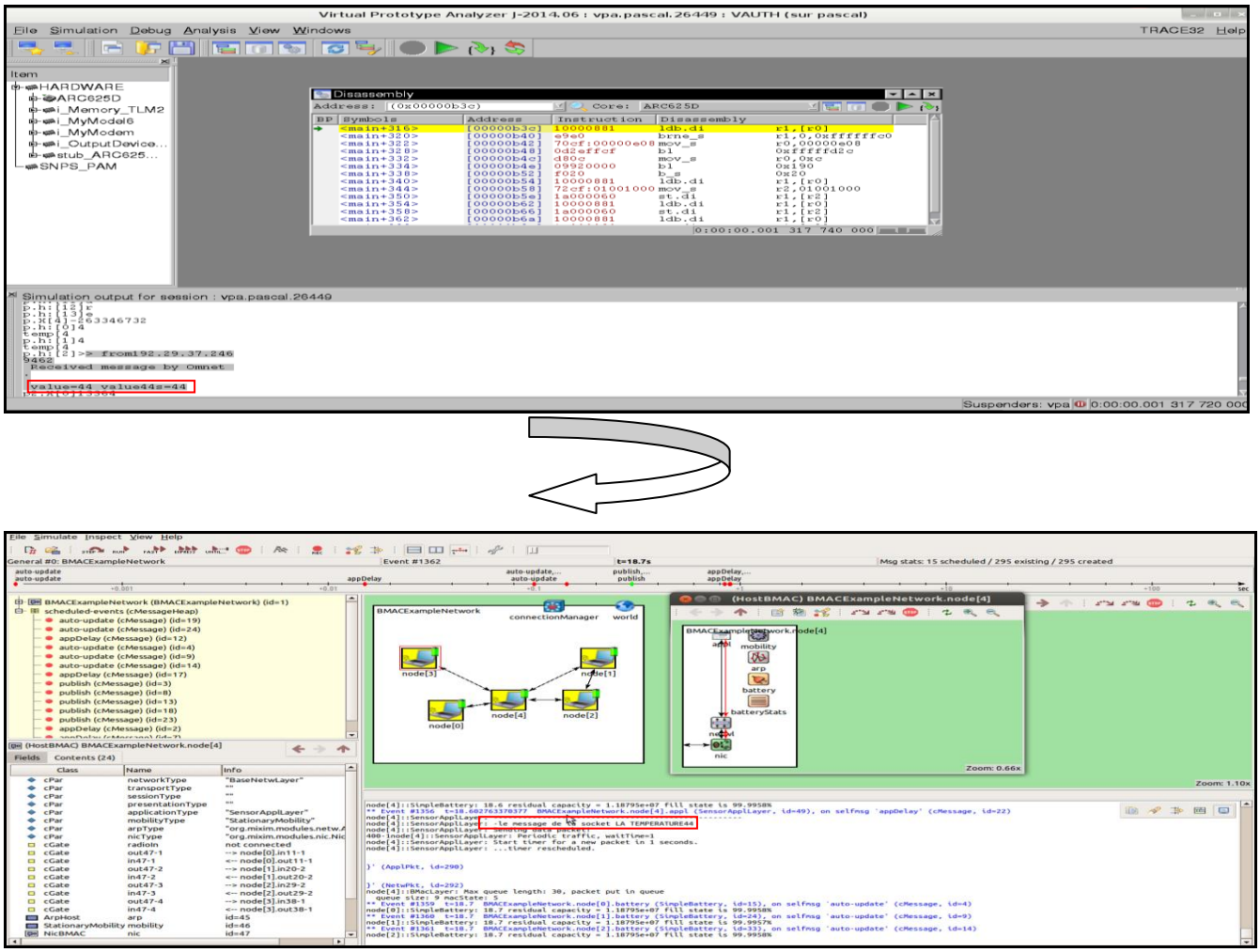

Figure 3. Simulation results

Discussion

In this study the two simulators have each one a local time and a local scheduler leading to a lack of timing coherency in the simulation results. In [6] a NS2-SystemC cosimulation technique based on a socket connexion is proposed with a fine grained synchronization mechanism between the two schedulers. In this approach significant simulation performance degradation are observed due to the frequent synchronization operations over the socket connexion. Techniques such as [5] allow the parallel execution of the two simulators to be controlled so as to maintain a coherent progress of time inside each simulator. Exchange of null messages required by this technique could be activated only on occurrence of events in one simulator that make sense for the other simulator. Such event is for example the transmission of the beacon from the coordinator node. On such event the simulator with the greater local time is suspended until local times are aligned.

To avoid time consuming synchronizations, a solution is to develop all the Hw/Sw/network components into a single modelling environment. This approach is used for example in [7] in which a channel model and protocol stacks are fully described in SystemC. In the event driven network simulator OMNEST [8], SystemC models can be directly included in a network simulation. This is achieved by extending the scheduler to be able to observe the SystemC events such that depending ono the type of the next timed event in the queues (SystemC or OMNEST) the corresponding model is activated. This mechanism avoids the synchronization operations of [6] and could be a convenient way to develop an efficient Hw/Sw/network cosimulation. However, tools like Virtualizer provide a lot of powerful facilities to help the designer in developing and debugging a Hw/Sw system. Thus a cosimulation framework where Virtualizer is embedded in a network simulator like OMNEST would be a powerful solution.

Concluding remarks

This work illustrates that in the context of IoT a cosimulation approach combining a SystemC-TLM virtual platform model of an Hw/Sw architecture node and a network model developed in a network simulator allows a precise analysis and validation of the Hw/Sw node in the early steps of the design process. Performance and power consumption analysis could be performed as well using the powerful facilities provided by Virtualizer allowing the architecture to be efficiently optimized at ESL while the real software code could be validated. In future wok we aim to introduce a synchronization mechanism between the two simulators and to evaluate/propose an IoT oriented middleware on top of a tiny RTOS for which a virtual platform approach makes sense for this Hw/Sw oriented objective

Acknowledgement

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About the Authors

Short Speakers' bio and photo

Wafa Khlif is an engineering student at central Nantes within the exchange program Erasmus mundus with the National School of Engineers of Sfax. She is currently a trainee at Plateforme Conception working on the above subject.

Hend Affes is currently a second-year PhD student at the University of Nice Sophia Antipolis. She is a member of the team "System level modelling and design of communicating objects" in LEAT laboratory. Her research is focused on the development of mechanisms to optimize the power for embedded system via Transaction Level Modeling (TLM).

Michel Auguin has currently a position of Director of Research at CNRS (Centre National de la Recherche Scientifique) in the group "System level modelling and design of communicating objects" of LEAT laboratory from University of Nice Sophia-Antipolis and CNRS in France. He is working on SoC system level design methodologies with a special interest on scheduling and power optimization for embedded systems. He is involved in several national and/or European collaborative projects dealing with these topics. Since 1995 he has been a staff member of several national research programs focusing on parallel architecture and SoC design.

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